Low Cost Design Techniques for Semiconductor Phase Shifters

RICHARD W. BURNS, MEMBER, IEEE, RUSSELL L. HOLDEN, AND RAYMOND TANG, MEMBER, IEEE

(Invited Paper)

***Abstract*—The design and performance of two microstrip semiconductor phase shifters operating at *S* band and UHF are described. The *S*-band diode phase shifter uses thick-film metallization on a 99.5-percent alumina substrate and uses series coupled diodes for the small bits and constant phase frequency switched line bits for the three large bits. The 4-bit UHF phase shifter uses eight p-i-n diodes mounted in a low dielectric constant microstrip circuit and operates at a power level of 8 kW peak, 240 W average, and has an average insertion loss of 0.7 dB. Phase and VSWR distributions on 800 units produced are also given. The characteristics of two new microwave semiconductor switching devices, the field-effect diode (FED) and the resistive gate switch are described. These devices operate with only a voltage change. Design and performance of an SP2T switch and 3-bit phase shifter using the field-effect diode are presented.**

I. INTRODUCTION

WORK on semiconductor phase shifters for phased arrays began in the late 1950's using the p-i-n diode as the control element. In those days phase-shifter costs were high because diodes were expensive and circuits generally were made using many machined parts. Over the years diode performance has improved with advances in silicon technology, and with the introduction of batch processing techniques [1], [2] diode prices have dropped significantly. At the same time circuit designers have gone to stripline and microstrip construction in order to decrease fabrication and assembly costs. Two such microstrip phase-shifter designs using p-i-n diodes are discussed in this paper. The first, a 5-bit *S*-band device, was fabricated on a 25-mil-thick alumina substrate with a dielectric constant of about 10. The second, a UHF 4-bit device, was built on a 1/8-in-thick stripline board with a dielectric constant of 2.55.

The last part of the paper describes work that has been done on RF semiconductor control devices which do not require current to switch. These devices show promise for cost reduction in phased arrays since the cost of present phased array antenna systems using p-i-n diode phase shifters is divided equally between the phase shifter and driver. These devices also have applications in airborne and arrays in space where prime power restrictions are severe. Development of two new RF control devices, the field-effect diode (FED) and the resistive gate switch, began in 1969. These devices switch with only a voltage change as contrasted with p-i-n diode switches which require two bias levels of opposite polarities with 25–100 mA of current required in one state. This paper describes the design and performance of several *L*-band devices which have been built using these new switches. While the present RF performance of these devices is not comparable with p-i-n diode devices, further improvements can be expected in the future much in the manner that p-i-n diodes improved over the years.

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The authors are with the Ground Systems Group, Hughes Aircraft Company, Fullerton, Calif.

II. *S*-BAND DIODE PHASE SHIFTER

The design of a miniature 5-bit diode microstrip phase shifter is described. This circuit has been optimized for low cost batch processing while maintaining a high degree of performance over a 12-percent bandwidth. This phase shifter is incorporated in a solid state transmit–receive antenna element module [3] which has been developed at Hughes Ground Systems.

The module requirements for this phase shifter were as follows:

center frequency	3.3 GHz;
bandwidth	12 percent;
average loss	1.75 dB;
number of bits	5;
phase-shift accuracy	±3°;
VSWR	1.5 maximum;
size	1 × 2 in;
average power	15 W.

A schematic diagram of the phase shifter is shown in Fig. 1. The 180, 90, and 45° bits are frequency compensated switched line circuits, and the 22.5 and 11.25° bits are series coupled loaded line circuits. Hybrid coupled sections were considered for the three large bits. The specified bandwidth required the use of either three branch hybrids or coupled line hybrids. These were discarded because of the large physical size of the three branch hybrid and the tight fabrication tolerances of the coupled line unit.

The 11.25 and 22.5° phase bits use series coupled loaded line circuits. These circuits use switched loading reactances spaced a quarter-wavelength along a transmission line (Fig. 2). Adjacent loading reactances are normally equal and are switched into a capacitive or an inductive state. Impedance-matched transmission for both stages is maintained by correctly choosing the impedance level of the transmission line section between diodes.

Shunt coupled loaded line circuits have been treated extensively in the literature [4], [5]. Very little attention has been given the series loaded circuit configuration mainly because of the difficulty in adjusting the amount of series loading in order to realize different bit sizes with

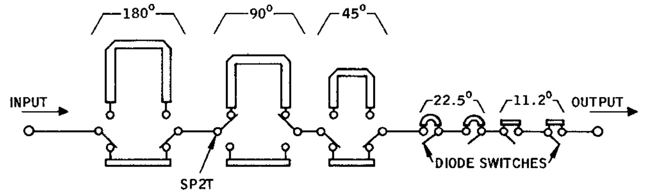


Fig. 1. Schematic diagrams of 5-bit micromin diode phase shifter.

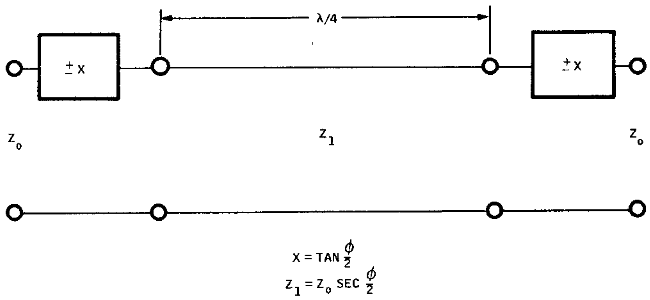


Fig. 2. Series coupled loaded line phase bit.

similar diodes. This problem is particularly difficult in micromin circuits where small capacitance p-i-n diode chips are used. These p-i-n chip diodes have a reactance which is typically 10–20 times the impedance of a 50-Ω line at S band, hence, will normally give a large mismatch loss when reverse biased. In order to prevent this large mismatch, each series mounted diode is shunted by a short length of high impedance transmission line as shown in Fig. 3. A capacitor is in series with each shunt line in order to prevent shorting out the diode bias. If the short length of transmission line around each diode is represented by a π equivalent circuit [6], the electrical equivalent circuit of a single diode switch can be drawn as shown in Fig. 4. When the diode is changed from forward to reverse bias, the reactance of the series element in the π network changes from a low inductive value to a high inductive value, respectively. In the special case when the capacitive reactance of the diode is much greater than the series inductive component, the equivalent circuit reduces to that of a short piece of high impedance transmission line. Also of interest is the forward biased case where the diode series inductance is zero. The equivalent circuit of the forward biased switch reduces to just two capacitors (B) in shunt across the line, or a shunt loaded line circuit.

Computer calculations have been run on the series coupled loaded line circuit. These calculations (Fig. 5) show that if the interconnecting transmission line between identical switches is reduced from the nominal quarter-wavelength by about 20 percent, a VSWR of less than 1.25 in both states can be realized over an octave bandwidth for a 22.5° phase bit.

Fig. 6 shows the results of a series of experimental circuits where the length of the transmission line around the diodes was changed in a uniform manner in a series of discrete steps. The experiment shows that fairly precise control of the nominal phase shift can be obtained by simply adjusting the length of the transmission line around

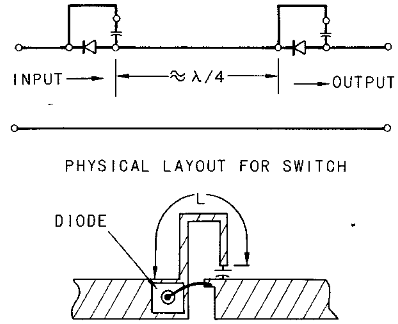
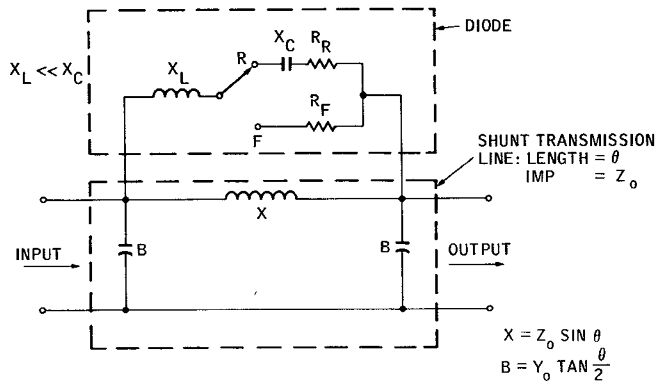


Fig. 3. Electrical equivalent circuit for the 11.25 and 22.5° phase bit.



TOTAL REACTANCE OF SERIES COMPONENT OF π NETWORK	
REVERSE BIAS	FORWARD BIAS
$X_T = \frac{X \cdot X_C}{X_C - X}$	$X_T = \frac{X_L \cdot X}{X_L + X}$
IF $= X_C >> X$ THEN $X_T = X$	IF $= X_L \rightarrow 0$ $X_T \rightarrow 0$

Fig. 4. Electrical equivalent circuit of series coupled switch.

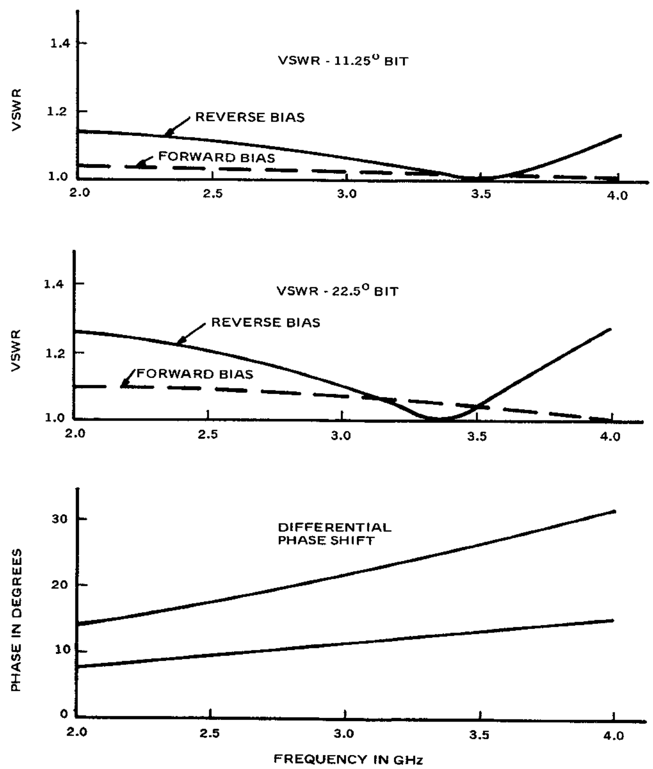


Fig. 5. Calculated performance for series coupled loaded line bits with 0.08-pF p-i-n diodes.

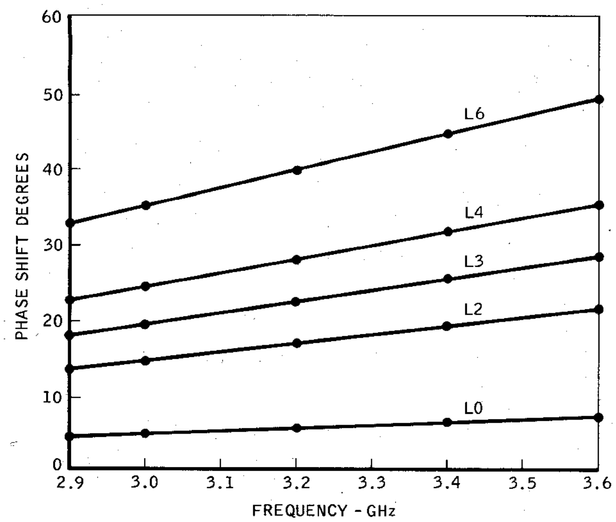


Fig. 6. Measured phase shift for small bit design.

the diode. The curves also show a phase-frequency slope which is proportional to frequency.

The most difficult parameter to achieve in the design of this phase shifter was a flat phase-frequency characteristic over the 12-percent bandwidth using switched line phase bits. Schiffman [7] sections can be used, but these require long delay lines on the order of at least two wavelengths for a 180° bit as well as 4–6-dB coupler sections [8] in the reference paths. Tight couplers are difficult to realize on thick film micromin microstrip circuits. A flat phase-frequency characteristic was achieved by compensating the reference path in the switched line bits with shorted quarter-wavelength loading stubs (Fig. 7). This loading allows the phase slope versus frequency characteristic for each reference path to be equal to the phase slope of the delay path; thus the net phase difference over the frequency band is constant. The normalized characteristic admittance (Y_0) of a stub required to give flat phase is related to the midband phase shift $\Delta\varphi$ by

$$Y_0 = \frac{2}{\pi} \cdot \Delta\varphi.$$

Thus, for a 180° phase bit, the normalized characteristic admittance of one stub must be 2 in order to give flat phase shift. Likewise, the admittance of a stub must be 1 for a 90° bit.

A photograph of the completed phase shifter is shown in Fig. 8. The phase shifter is fabricated on a 0.025-in-thick 99.5-percent alumina substrate and measures 1 by 2 in. Thick film gold conductors and thick film blocking and bypass capacitors are used throughout. Electro-Science Lab's 8831 gold is used for conductors, and the capacitor dielectric is ESL 4310. The bias bypass capacitors function in a manner similar to that of a feedthrough capacitor; that is, the quarter-wavelength bias leads pass over the bottom plate of the capacitors which are wrapped around the substrate edge to make contact with the ground plane. This method minimizes series inductance and provides an RF ground for the bias leads. Blocking capacitors are

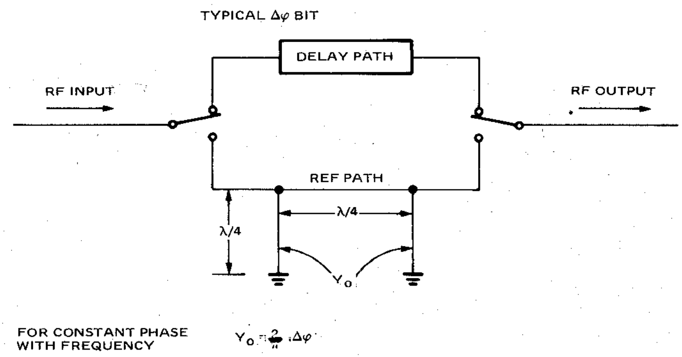


Fig. 7. Method of obtaining a flat phase frequency characteristic for the switched line phase bits.

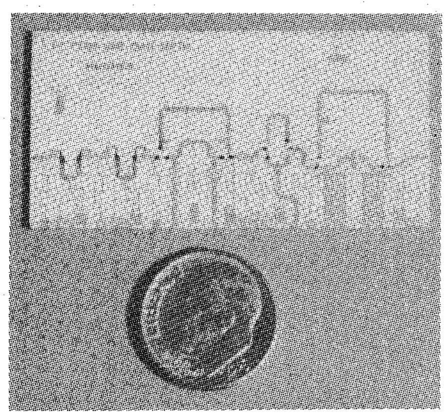


Fig. 8. Photo of 5-bit micromin phase shifter fabricated on a 1- × 2-in alumina substrate. The three long bits are frequency compensated switched line circuits and the two short bits use series coupled loaded line circuits. A total of 16 p-i-n diodes are used in the device.

incorporated in the frequency compensating stubs of the three larger bits. These capacitors are required to prevent shorting out the dc bias in the reference paths. Two compensating stubs separated by a quarter-wavelength are used in the 180 and 90° bits. Only one phase compensating stub was required for the 45° bit.

There are four diodes in each of the three larger bits, and two diodes in each of the two smaller bits for a total of sixteen diodes in the complete phase shifter. The diodes, Hewlett Packard Associates' 5082-0012, have a reverse bias capacitance of less than 0.1 pF at 50 V and a dc breakdown voltage of 200 V.

Fig. 9 shows the dc bias circuitry for the phase shifter. In the 45, 90, and 180° bits the diodes in each path are biased in series, with the dc polarity of the delay path diodes being opposite to that of the reference path diodes. This arrangement allows for the minimum number of bias return leads and necessitates the use of only one bias control lead per bit. Phase switching is accomplished by simply changing the polarity of the control voltage. The bias requirement is therefore approximately ±1.5 V at 50 mA. The two diodes in each of the two smaller bits are in dc parallel and operate at a level of 0 and +0.75 V at 50 mA.

The measured performance of the completed phase shifter is shown in Figs. 10 and 11. The input VSWR for

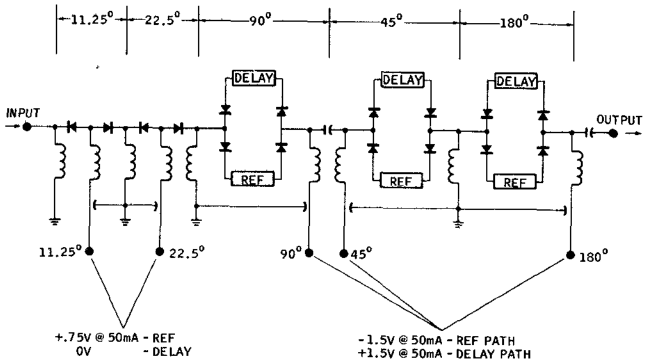


Fig. 9. Bias circuitry for the 5-bit phase shifter. The diodes in the switched line bits are biased in series and the diodes in the loaded line bits are biased in parallel.

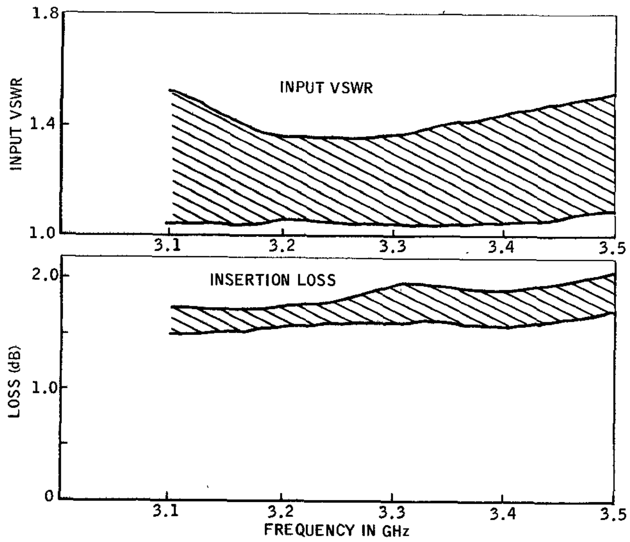


Fig. 10. Measured VSWR and insertion loss for 5-bit micromin S-band phase shifters

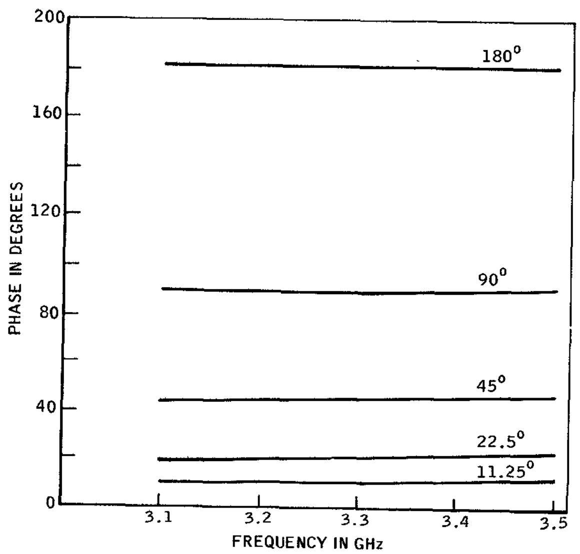


Fig. 11. Measured phase shift for 5-bit micromin S-band phase shifter.

all 32 phase steps is less than 1.5 over the frequency range of 3.1–3.5 GHz. Average insertion loss is 1.75 dB with the maximum loss being less than 2 dB over the same frequency range. The loss with all diodes replaced with wire bonds was 1.1 dB. Phase-shift accuracy of any step is within a few degrees of nominal over the entire band.

III. HIGH POWER UHF MICROSTRIP DIODE PHASE SHIFTER

High power p-i-n diode phase shifters have used large numbers of diodes in order to achieve high power capacity [4], [9], [10]. Circuits in the past have generally used coaxial transmission lines which require many expensive machined parts. This paper describes the design of a 4-bit high power UHF diode phase shifter which has been optimized for low loss at high power levels. In order to minimize production costs, the phase shifter uses only eight diodes mounted in a relatively simple microstrip circuit.

The design goals for this phase shifter were as follows:

center frequency	400 MHz;
bandwidth	5 percent;
maximum loss	1.0 dB;
phase-shift accuracy	±11°;
VSWR	1.3 maximum;
peak power	4 kW;
duty factor	3 percent;
pulse length	300 μs;
bias per bit	200 mA forward; −100 V reverse.

A schematic circuit diagram of the phase shifter is shown in Fig. 12. The phase shifter incorporates a combination of bit designs. The 90 and 180° bits are hybrid coupled circuits and the 22.5 and 45° bits are shunt coupled loaded line sections. Each bit uses two p-i-n diodes made by Unitrode Corporation. The diodes, type UM 4000, have a forward bias series resistance of less than 0.3 Ω at 100 mA and a reverse bias series resistance of less than 0.6 Ω at −100 V. The capacitance is approximately 2.0 pF and the dc breakdown voltage is 800 V.

The most stringent design goal for this phase shifter was to maintain low insertion loss at a peak power level of 4 kW with only −100 V of reverse bias. The diodes in the 180° bit are mounted at a 25-Ω impedance level. At a power level of 4 kW the maximum RF voltage across these reversed biased diodes is about 630 V. Ideally, a diode switch is reverse biased to a voltage level that is at least equal to the peak forward excursion of the applied RF voltage, 630 V in this case. This is done in order to avoid operating the diode in the high resistance region near zero bias. When the peak excursion of the RF voltage swings into this region, with the diode in reverse bias, high level limiting occurs and the loss increases [9], [11]. As the operating frequency is decreased to the UHF region, this limiting effect becomes more pronounced since the diode series resistance, near zero bias, varies inversely as the square of the frequency [12]. In this design, high level

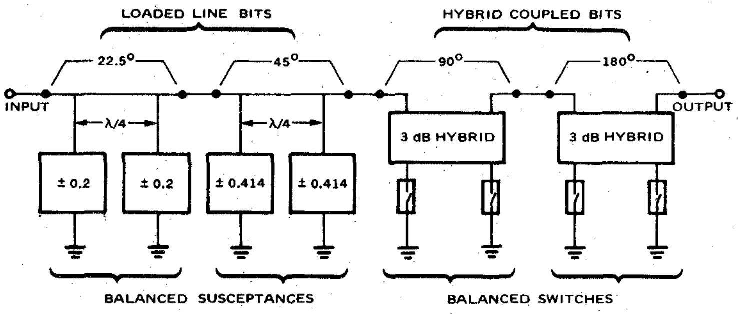


Fig. 12. Schematic diagram of 4-bit UHF diode phase shifter.

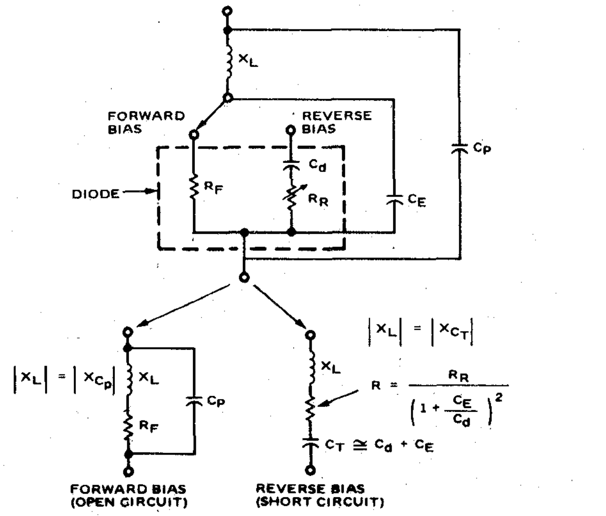


Fig. 13. Electrical equivalent circuit for 180° switch in phase shifter. The diode is shunted by a lumped capacitor C_E in order to increase the peak power capacity.

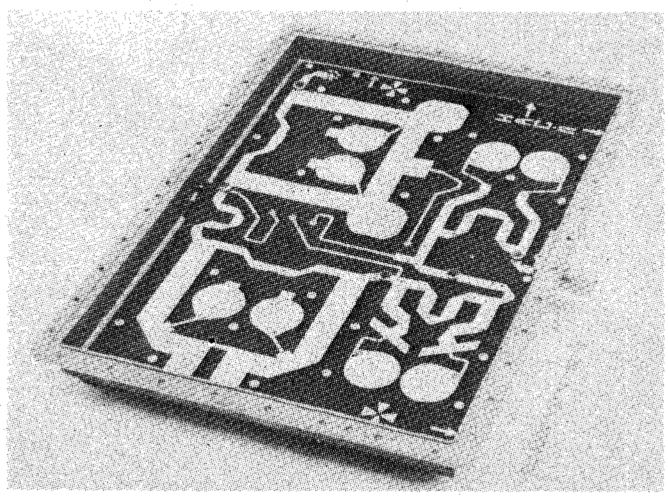


Fig. 14. UHF diode phase shifter with cover removed. A microstrip circuit on a low dielectric constant circuit board is used.

limiting is minimized by shunting the 2-pF diode C_d with an external 14-pF high-Q capacitor C_E, as shown in Fig. 13. This combination effectively lowers the equivalent reverse bias series resistance by a factor of $(1 + C_E/C_d)^2$ or about 64. This reduction of series resistance improves the high level limiting characteristic of the diode. Additionally, a substantial cost reduction benefit was realized in that the capacitance tolerance of the diode is not critical and a variation on the order of ± 20 percent could be tolerated while maintaining phase-shift accuracy.

The 25-Ω capacitive reactance of the diode and shunt capacitor combination X_{CT} is series resonated with the inductive reactance X_L to produce a short circuit condition in the reverse bias state (Fig. 13). An open circuit condition is obtained in forward bias by parallel resonating X_L with X_{C_p}.

Fig. 14 shows a photograph of the microstrip phase-shifter circuit. The 3-dB two branch hybrids used in the 90 and 180° bits, incorporate transformers which lowers the 50-Ω main transmission line impedance to 25 Ω at the diode switches. The switches are mounted directly on the coupled ports of the hybrids in order to conserve space.

Loaded line sections are used for the two smaller bits in order to keep the circuit area to a minimum. The switches for these bits are coupled to the main line through quarter-wavelength lines. The impedance level of these lines is adjusted to yield shunting susceptances of $\pm J.2$ and $\pm J.414$ for the 22.5 and 45° bits, respectively. Each pair of susceptances are quarter-wavelength spaced along the transmission line, which is adjusted for low VSWR across the band.

The circuit was fabricated on a 1/8-in-thick polyphenelene oxide (PPO) laminate using conventional print and etch techniques. This board has a dielectric constant of 2.55 and a loss tangent of 0.0006 at UHF. The circuit board is mounted in a watertight die cast housing which also serves as a finned heat sink for the diodes. In order to obtain good heat transfer to the heat sink, each diode is mounted on a large copper stud which is threaded into the housing (Fig. 15). The base of the stud makes contact with the circuit ground plane while the diode extends through the board to make contact with the etched circuit. The four bits are dc isolated from one another by 100-pF button mica blocking capacitors. The total loss contributed by the five capacitors was less than 0.1 dB. Mica feed-through capacitors are used to bypass the bias control lines. A photograph showing the exterior of the completed phase shifter is shown in Fig. 16. Type N connectors were used on the input and output of the phase shifter.

Fig. 17 shows the measured performance for a typical

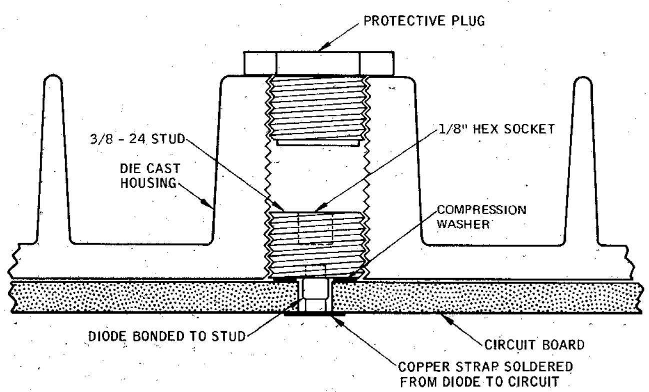


Fig. 15. Mounting detail for diodes. Each diode mounted on a threaded post is screwed into the body of the housing.

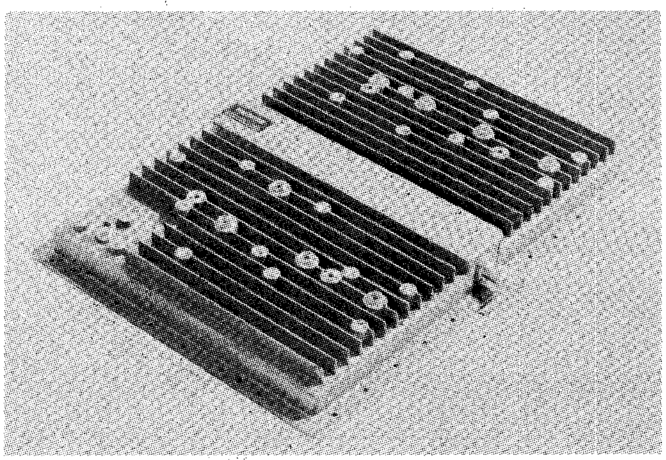


Fig. 16. Exterior view of UHF shifter. Overall size is 20 by 14 by 2.2 in thick and the weight is 13 lbs.

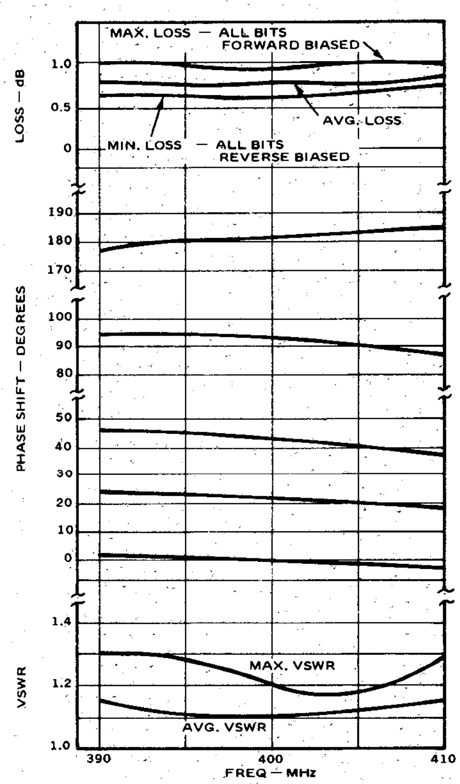


Fig. 17. Measured insertion loss, phase shift, and input VSWR for a typical phase shifter.

phase shifter. The maximum insertion loss is under 1 dB, with the average loss about 0.75 dB over the band for all phase steps. The measured insertion loss for the phase shifter with all of the diodes removed was about 0.5 dB, hence, the loss contributed by the diodes varies from 0.1 dB with all diodes reverse biased to about 0.5 dB with all diodes forward biased. A flat phase-shift characteristic over the operating frequency range was required. This requirement was met with the measured phase deviation being only $\pm 8°$ for all 16 phase steps, from 390–410 MHz. Input VSWR is less than 1.3 over the same frequency range. Although the peak power requirement was 4 kW, the phase shifter was tested to a peak power level of 8 kW with a 3-percent duty factor and a 300-ms pulse length. As the power was increased from a low level to the 8-kW level, the measured increase in insertion loss was less than 0.1 dB for all phase steps.

Following the design phase of this program, 800 phase shifters were fabricated and tested. Standard tolerance components were used throughout: diode capacitance ± 20 percent, circuit board thickness ± 0.004 in, commercial grade capacitors, castings, and connectors. With these tolerances in mind, provision for insertion phase trimming of the production units was provided by adding a small stub to the circuit which could be trimmed by removing a small piece of the copper circuit. Fig. 18 shows the measured phase error distribution for all 16 phase steps, including both insertion and differential phase shift for the entire 800 units when compared to a standard phase reference. The phase error for 81 percent of the total is within 6° of the reference, while the remaining 19 percent is within 11°. This phase accuracy was achieved by insertion phase trimming only 10 percent of the total production run.

Fig. 19 shows the input VSWR distribution of the 800 phase shifters for all phase steps. The VSWR for 98 percent of the total steps is less than 1.2:1 with the remaining 2 percent less than 1.3:1.

The maximum insertion loss for all 800 units was less than 1 dB.

IV. VOLTAGE CONTROLLED SWITCHES

Semiconductor diode switches and phase shifters reported in the past have used either a p-i-n or varactor diode as the control element. The varactor has primarily been used for analog phase-shifter applications and its use has been limited to low power levels due to the modulation of the nonlinear capacitive–voltage characteristics with high power. The p-i-n diode has extended the power handling capabilities of diode phase shifters up into the kilowatt region. The major drawback to p-i-n diode switches is that they require two bias levels of opposite polarities with 25–100 mA of drive current required in one state. The net result is that in a large phased array, the cost of the drivers is very expensive, typically the same order as the phase shifters.

Two new RF switching devices, the "FED" and the "resistive gate switch" do not require current to switch.

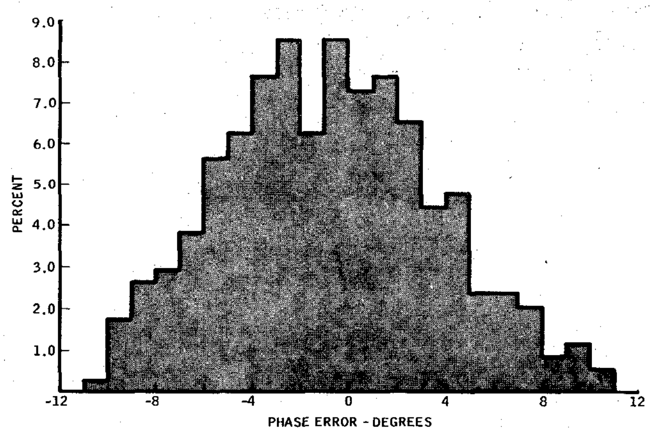


Fig. 18. Phase error distribution for 800 production units. These errors include both insertion and differential phase shift for all 16 phase steps.

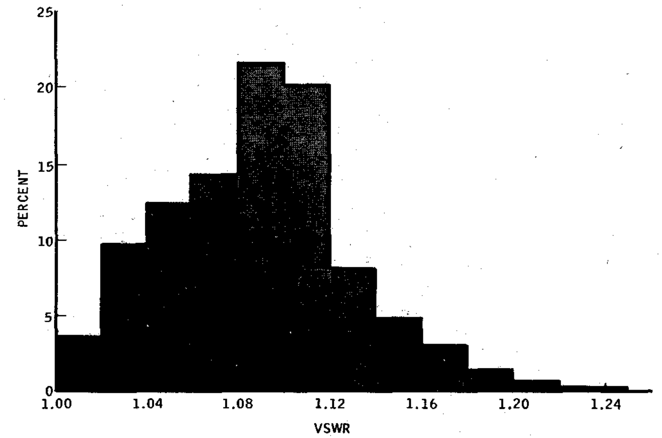


Fig. 19. VSWR distribution for all 16 steps in 800 production units. The VSWR is less than 1.2:1 for 98 percent of the units.

These devices switch with only a voltage change. In addition, they can operate directly from computer logic levels, thus eliminating the requirement for an expensive driver, and they require holding power on the order of microwatts compared to 0.1 W for a conventional p-i-n diode switch. This reduction in control power is important since the prime control requirements for a phased array with several thousand elements is very large, typically on the order of several kilowatts. This problem is particularly severe in airborne or space applications. Phased array control power can be reduced to a level of several watts by using devices which do not require current to switch.

Work on semiconductor voltage controlled phase shifters began at Hughes Ground Systems in 1969. Work initially began on phase shifters using a field-effect diode which operates as an RF switch with a small voltage change. Recently, Hughes has developed the resistive gate switch [13] which also operates with only a voltage change, and in addition, it offers the promise of much higher RF power operation than the FED. Work on components using this new device is currently under way.

A. Comparison of RF Switching Devices

The FED and the resistive gate switch are compared with other microwave semiconductor switching devices in

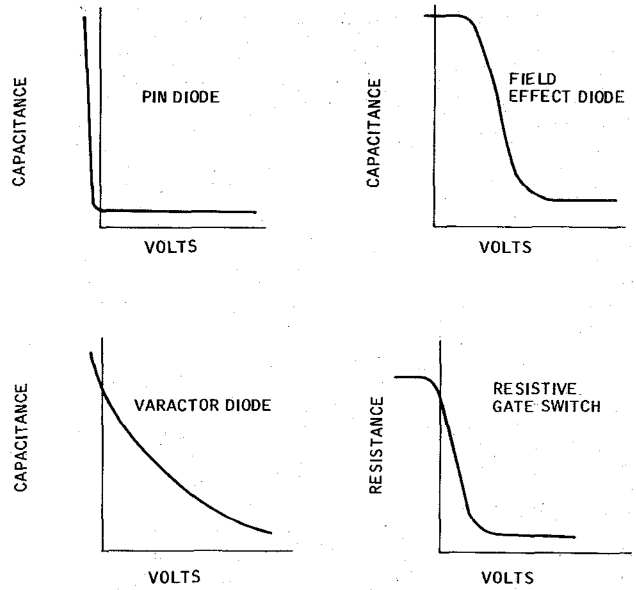


Fig. 20. Characteristics of microwave semiconductor control devices.

Fig. 20. The p-i-n diode has a constant capacitive–voltage characteristic and is useful for power levels into the kilowatt range. The p-i-n diode switch requires two bias levels of opposite polarity. In one bias state, the p-i-n diode draws about 50 mA at 1 V and in the opposite state, 1 μA at -100 V. In a large phased array with thousands of elements, the driver power requirement including the driver may be in the range of 2–5 kW. The varactor does not require forward bias but has a nonlinear capacitance–voltage characteristic with high RF power. This characteristic causes the RF signal to be distorted at high power levels. The FED has two regions where the capacitance is independent of the voltage and, therefore, is capable of much higher power than the varactor diode. The major drawback to the FED is that it has a very fast response time and essentially follows the RF voltage swing. RF peak power capacity is, therefore, limited by the allowable RF swing in the two flat capacitance regions. The resistive gate switch has two regions where the resistance is independent of voltage. The resistance of these two regions is different by a factor of typically 500–1000. Because of its unique construction there is a capacitance associated with each constant resistance region, hence, each has a time constant. During the fabrication process, these time constants can be adjusted so that the device will change state within the required switching time interval, and at the same time be much slower than the period required for an RF cycle. This means that the resistive gate switch is slower compared with the varactor or FED, but it can handle much higher peak powers because the RF voltage can overswing the "static" voltage regions of the device with no effect. Since the bias voltage controls the resistance of the device, large variations of bias voltages on the order of ± 10 percent can be tolerated with no change in phase shift. The switching time of this device is still in the order of 10 μs.

B. Description of Resistive Gate Switch

The resistive gate switch is a new microwave control device. The structure of the device is planar and has only one layer of metallization. This minimizes construction cost because the device can be built by using processes which can be related very closely to standard MOS processing.

The basic switch structure (shown in Fig. 21) consists of a highly resistive silicon N substrate covered by an insulating layer of SiO_2 and a thin highly resistive gate film of boron-doped polysilicon. An interdigitated source and drain electrode structure is deposited on top of the resistive gate structure. As a result, the high resistivity gate covering the channel region is permanently connected to the source and drain electrodes, and the entire source–gate–drain structure is isolated from the substrate.

The device operates in the following manner. In the "OFF" condition the resistive gate is biased at a level of 0 V in the flat band condition with respect to the substrate. No surface channel exists in this case, and the source to drain leakage impedance is determined by the high resistance R_g of the resistive gate and the small capacitance C_{SD} between the interdigitated source and drain electrode structure as shown in Fig. 22.

In the "ON" condition, the gate assembly is biased to a level of +20 V and forms a conducting channel in the silicon substrate by inverting the surface at the silicon–silicon dioxide interface. The carriers are supplied by the implanted regions which surround the source and drain structure. The impedance of the conductive path is now dominated by the series combination of source to channel capacitance C_{SC}, channel resistance R_{CH}, and channel to drain capacitance C_{CD}, as indicated in Fig. 22. Since the gate assembly is voltage controlled there is no dc conduction path, therefore, no bias current is required to hold the device in either the "ON" or the "OFF" condition.

C. Components Developed Using FED's

The FED was developed for the specific purpose of obtaining phase shift at microwave frequencies without the use of forward bias. A measured capacitance and series resistance characteristic for the device is shown in Fig. 23. At zero bias, the capacitance is about 10 pF with a series resistance of about 3 Ω. At a voltage of about 3 V both the capacitance and resistance start to decrease reaching a minimum value at a bias of about 8 V. Both the resistance and capacitance are independent of voltage out to the breakdown voltage which is typically 25 V.

Several circuits incorporating FED's have been developed and fabricated by Hughes Ground Systems. Fig. 24 shows a photograph of an L-band SP2T FED switch etched on a 1 × 1-in alumina microstrip substrate. An electrical equivalent circuit for the switch is shown in Fig. 25. This switch uses two shunt mounted FED switches spaced a quarter-wavelength distance from a common junction. When one switch is biased "OFF" to a short

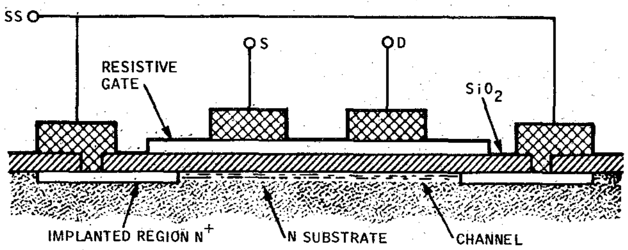


Fig. 21. The resistive gate switch. This device uses a planer structure and is built using processes which are closely related to MOS technology.

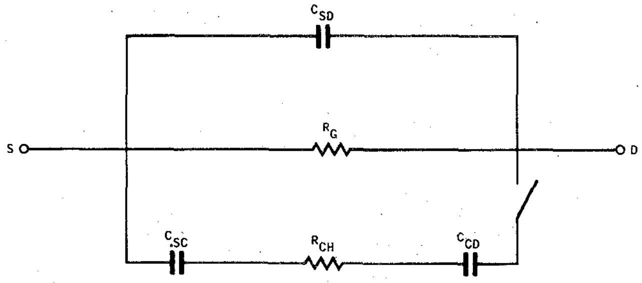


Fig. 22. Electrical equivalent circuit for the resistive gate switch.

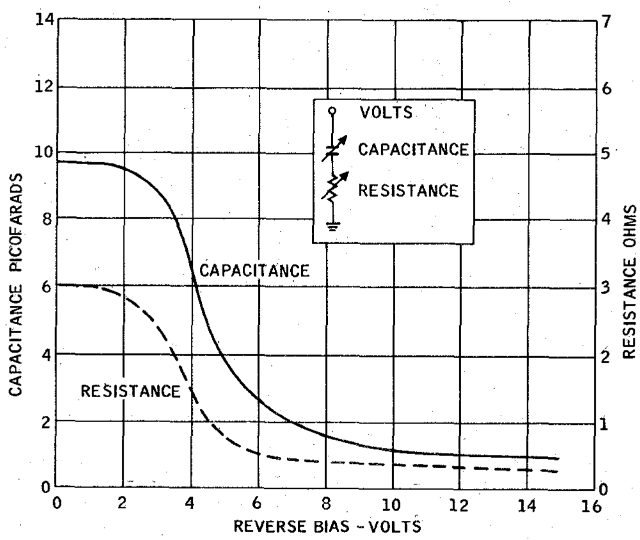


Fig. 23. Measured resistance and capacitance for the FED at L band.

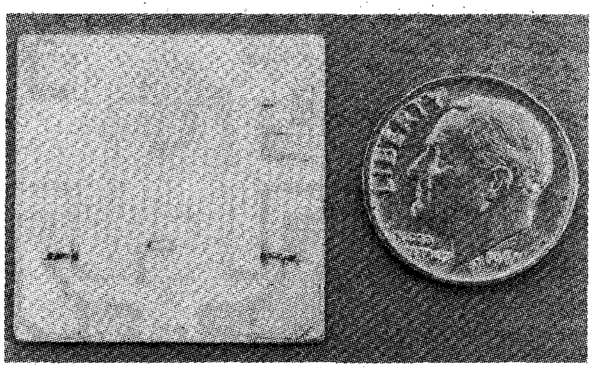


Fig. 24. Photo of SP2T FED switch. The switch is fabricated on a 1- by 1-in alumina substrate.

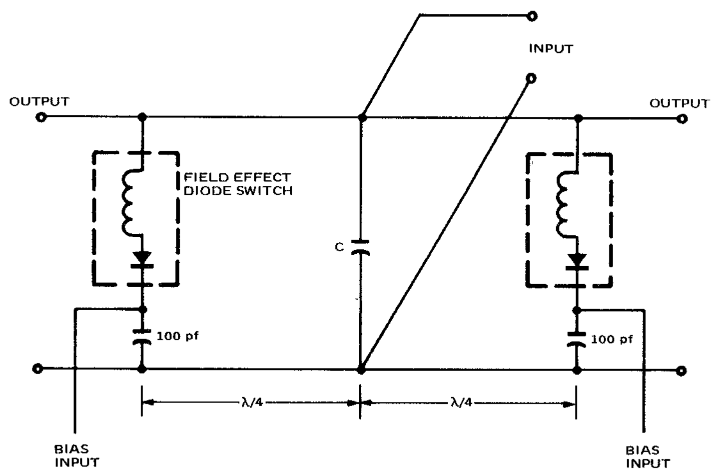


Fig. 25. Electrical equivalent for SP2T FED switch.

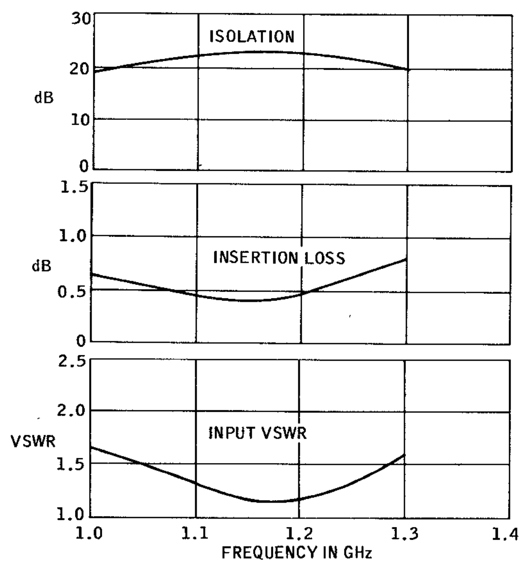


Fig. 26. Measured performance of SP2T FED switch.

circuit condition, the other is biased "ON" to a pass condition.

Fig. 26 shows the measured performance of the switch. The isolation of the "OFF" arm is greater than 20 dB over a 15-percent bandwidth. Insertion loss from the input to the pass arm is less than 0.5 dB and input VSWR is less than 1.5 over the same bandwidth.

An *L*-band phase shifter using the FED in hybrid coupled bits has also been designed and built. During this effort the theoretical performance of the two branch hybrid phase bit was compared with a rat race ring hybrid phase bit. The performance of the two branch hybrid and the rat race ring have been compared by Reed and Wheeler [14] who showed that the rat race ring has about twice the usable bandwidth of the two branch hybrid when all ports are terminated in matched loads. When these circuits are used as phase-shifter bits, highly reflective balanced diode switches are connected to the equal split ports. In addition the rat race ring requires an additional 90° line section in one coupled port in order that the reflected signals from the switches will cancel at the input port and add at the output port. The performance of the two branch hybrid and rat race ring circuit used as phase-shifter bits were analyzed using the circuit models of Fig. 27. The calculated input VSWR, loss, and phase shift are shown in Figs. 28–30. Idealized 180° switches (zero loss and 180° of differential phase shift over all frequencies) were used in these calculations. A variable line length was used between the switch and hybrid because it was found that the electrical spacing between the switch and hybrid affected phase error and input VSWR off of band center. Fig. 30 shows that the two branch hybrid has minimum phase error for a $\lambda/8$ spacing between switch and hybrid. A circuit loss of 0.2 dB/λ was assumed for all $Z_0 = 1$ lines and for all other lines, the attenuation constant was assumed to vary proportional with the square root of the normalized impedance [15].

A comparison of the two circuits shows that the rat race

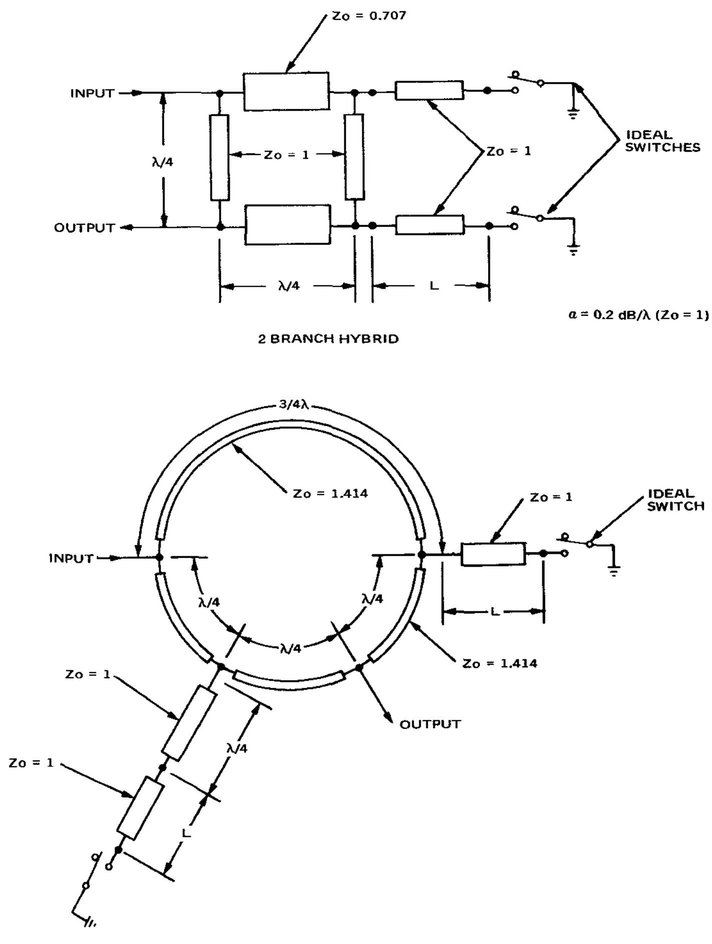


Fig. 27. Electrical equivalent circuits for 2 branch hybrid and rat race ring phase bits.

ring has approximately twice the VSWR bandwidth and less loss over a 10-percent bandwidth than the two branch hybrid. The two branch hybrid has less loss only near band center.

Fig. 31 shows a photo of an L-band 3-bit hybrid coupled FED phase shifter etched on an 8- × 9- × 1/16-in-thick teflon fiberglass microstrip circuit board. The phase shifter uses a hybrid coupled ring for the 180° bit. The 90 and 45° bits are combined on the second hybrid using a radial spoke design (Fig. 32). The FED is mounted at the end of each transmission line and is strap bonded to a 100-pF bypass capacitor which electrically puts the FED at RF ground. The bypass capacitor serves a double function in that it allows the dc bias to be applied to the FED without RF power loss. With reference to Fig. 32, the two stubs $L1$ and $L2$ are joined at a common junction. The impedance and length of the line $L1$ is adjusted so that when the FED bias is changed, a susceptance of $\pm J.435$ is presented at the common junction. The impedance and length of $L2$ is adjusted to present $\pm J.235$ at the same junction. Taking all combinations of the two independent steps gives four steps of $-J.67, -J.2, +J.2, +J.67$. This gives four reflection phase steps in increments of 45°. Figs. 33 and 34 show the measured performance of the phase shifter. Average loss is about 1.8 dB, and the average VSWR is less than 1.5 over a 15-percent bandwidth. Phase shift is within ±3° for any step at midband.

V. CONCLUSIONS

Low-cost construction designs have been described for a UHF and S-band p-i-n diode phase shifter for phased arrays. Characteristics of two new voltage controlled switching devices which do not require current to switch are also described. Measured results of an L-band switch and phase shifter built using an FED are given. A program sponsored by Naval Ship Systems Command is currently under way to build an S-band 4-bit phase shifter using the resistive gate switch. These new devices are attractive for cost reduction of future phased array systems since they greatly simplify driver design and also save on prime power requirement.

ACKNOWLEDGMENT

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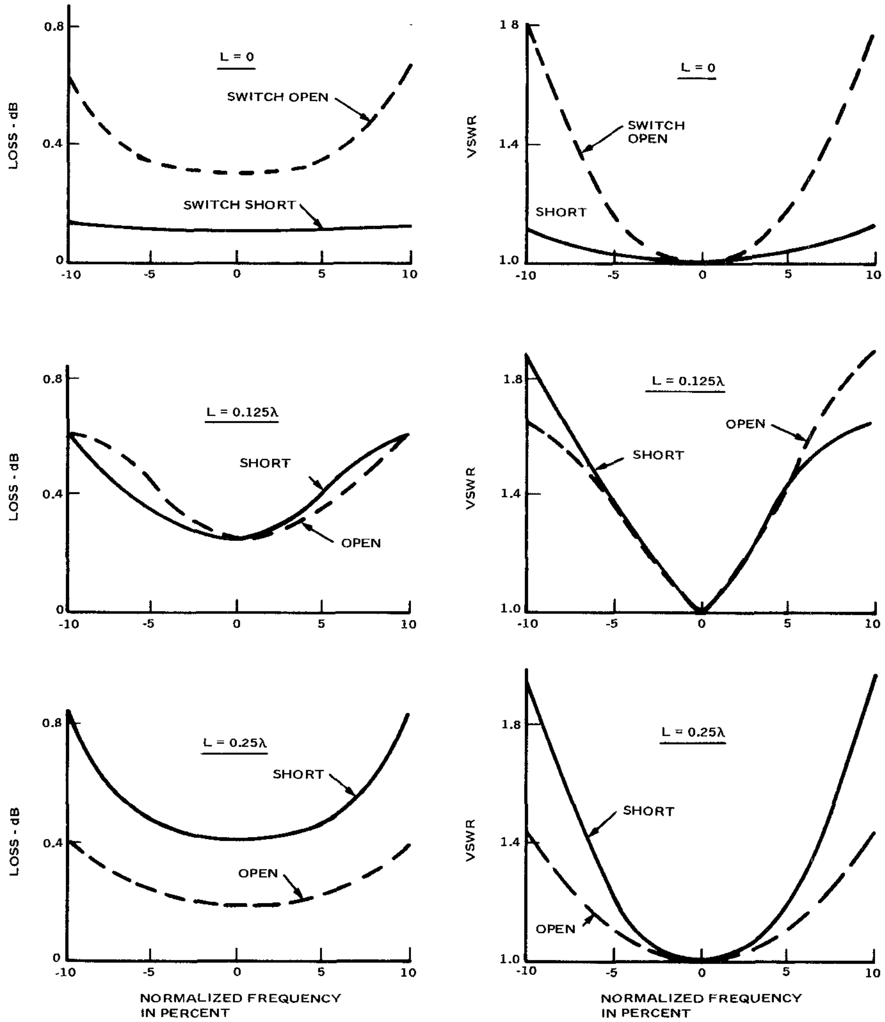

Fig. 28. Calculated loss and input VSWR for 180° phase bit using a two branch hybrid.

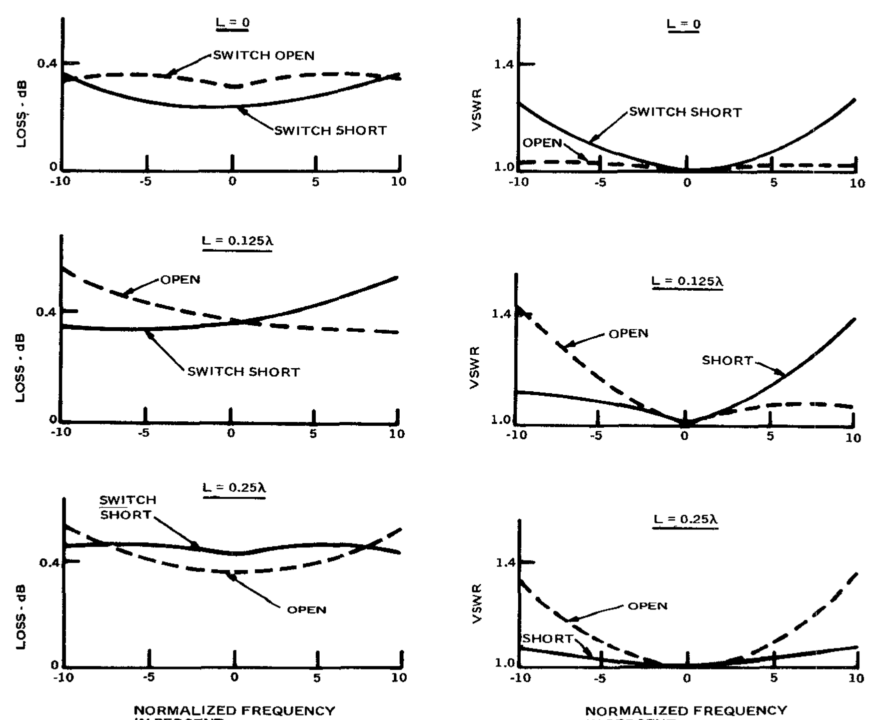

Fig. 29. Calculated loss and input VSWR for 180° phase bit using a rat race ring hybrid.

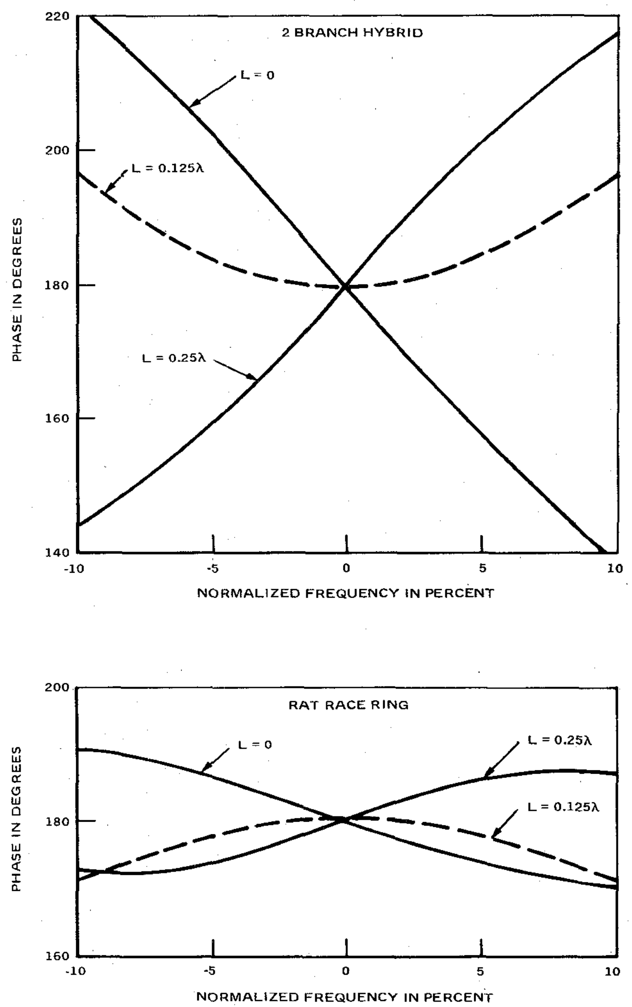

Fig. 30. Calculated differential phase shift for 180° phase bit using a two branch hybrid and rat race ring. Phase error depends strongly on the electrical distance between the hybrid and switches.

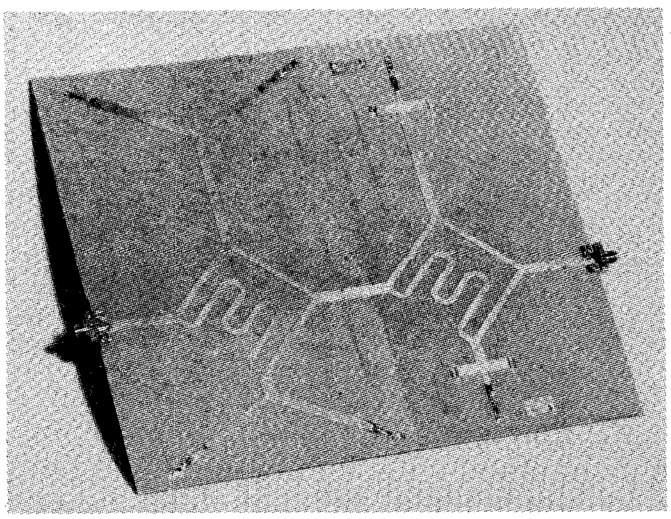

Fig. 31. 3-bit L-band FED phase shifter.

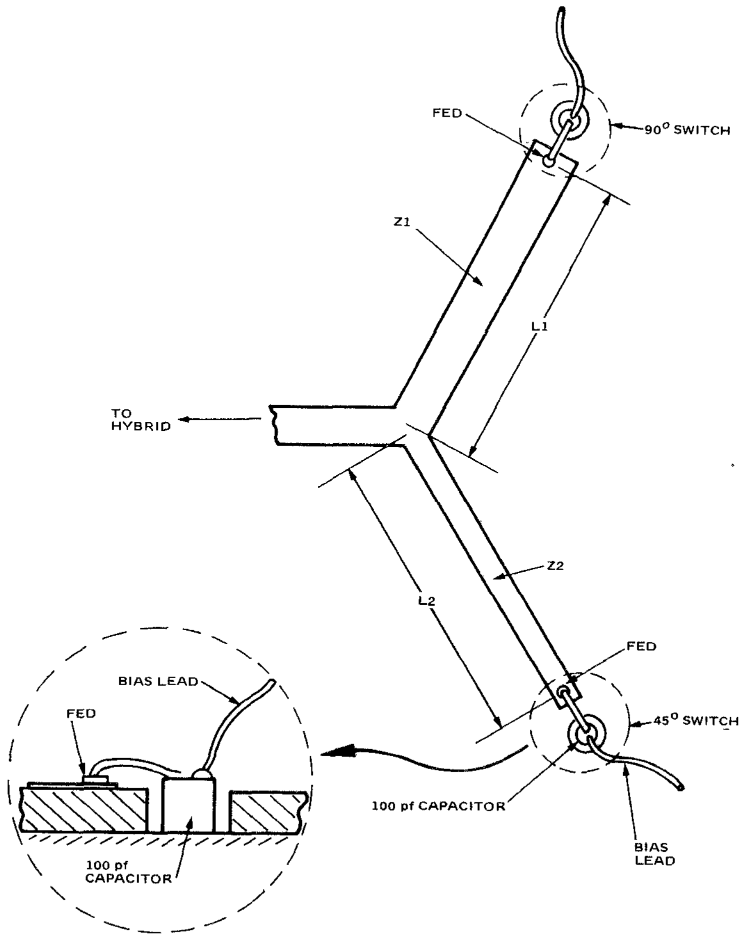

Fig. 32. Radial spoke design for 45 and 90° bit FED phase shifter.

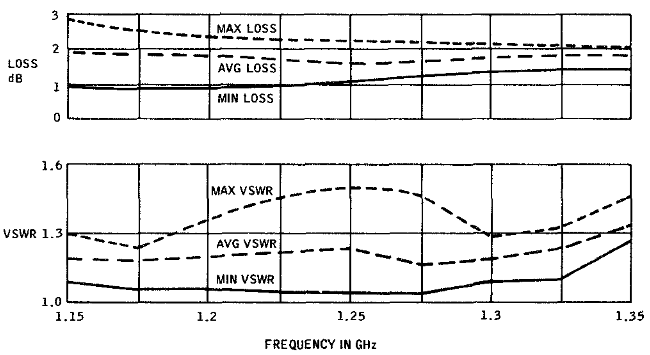

Fig. 33. Measured loss and VSWR for 3-bit FED phase shifter.

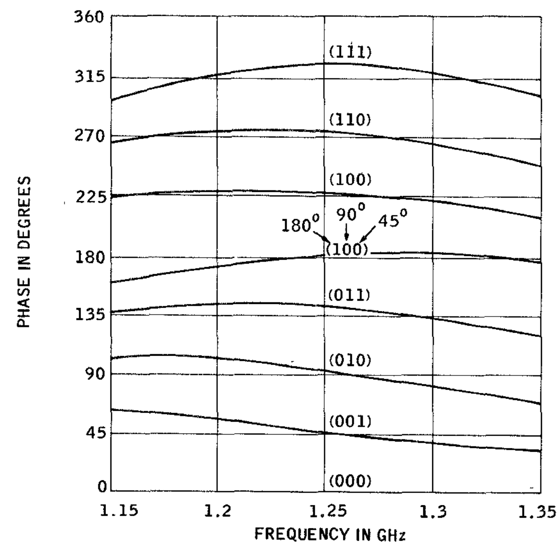

Fig. 34. Measured phase shift for all eight steps in 3-bit FED phase shifter.

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A Low Cost P-I-N Diode Phase Shifter for Airborne Phased-Array Antennas

FRANKLIN G. TERRIO, RONALD J. STOCKTON, AND WAYNE D. SATO

***Abstract*—This paper presents a description of a p-i-n diode phase shifter that was designed for low cost production for use in *X*-band phased-array systems. The phase shifter is designed to make maximum use of photoetched circuit components and low cost materials, and is well suited for assembly on a fully automated assembly line. The salient features of this phase shifter are a printed-circuit transmission structure and inexpensive RF connectors that are integrated into the circuit package. The microwave performance characteristics are generally superior to those of equivalent devices; a useful band width of 40 percent with an average insertion loss of 1.6 dB has been demonstrated with 3-bit units.**

INTRODUCTION

THE primary deterent to the use of phased arrays in airborne radars has been their cost. In particular, the several thousand phase shifters and driver circuits needed in a typical airborne X-band radar represent a significant fraction of the total phased-array cost. A phase shifter that is simple and suitable for automated production, and that offers significant reduction in both the cost and weight of phased arrays is described in this paper.

In airborne phased-array applications p-i-n diode phase shifters possess important advantages over ferrite devices; among these are light weight, temperature insensitivity, repeatable insertion phase characteristics, simple driver requirements, and high switching speed. The p-i-n diode phase shifters have a further important advantage in that production techniques can borrow heavily from integrated circuit production technology with its present high degree of automation. For the mass production of phase shifters it has been established through cost analysis that the lowest unit cost is achieved through manufacture with automated production lines, with testing limited to the unit level only.

Many important radar system applications require the use of a linearly polarized antenna. The phase shifter described in this paper, because of its simplicity, low cost, and light weight, has been developed for such an antenna requirement. The phase-shifter design can also be extended to a version that provides circular or variable polarization.

Although it is recognized that the driver and the array logic circuits that are an essential part of any practical array system will figure significantly in the total antenna cost, the problem of producing these circuits is not considered in this paper. In airborne phased arrays, the comparatively simple driver requirements of p-i-n diode phase shifters permit the drivers to be grouped together behind the array as integrated circuits. Because of the resultant simplification of the interconnections, this configuration is more cost effective than one in which individual drivers are placed at each phase shifter. Consequently, in the phase-shifter design described here, the drivers do not form a part of the phase-shifter package.

PHASE-SHIFTER CONSTRUCTION

In common with most X-band p-i-n diode phase shifters, this unit consists of several cascaded digital phase-shifting stages. Each stage provides one phase bit of control; the number of stages then determines the fineness of phase control possible. In typical phased-array applications

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F. G. Terrio and R. J. Stockton are with the Hughes Aircraft Company, Culver City, Calif. 90230.
W. D. Sato was with the Hughes Aircraft Company, Culver City, Calif. 90230. He now has his own business in Hilo, Hawaii.